

# MS-7688

ATX

Ver: 0A

## CPU:

INTEL -HAVENDALE/Lynnfield/Clarkdale LGA 1156

## System Chipset:

INTEL-IBEXPEAK PCH P55

## OnBoard Chipset:

Clock Gen:IDT 9LRS4116AKLFT

LAN:RTL 8111DL 10/100/1000 NIC X 2

SIO:FIN71889ED (LAA)

Flash ROM: 32 Mb SPI (CHIP)

## Main Memory:

DDRIII (1066/1333MHz) \* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 2

PCI Express (X1) Slot \* 2

PCI Slot \* 2

## PWM:

Controller:uP6218 ( 8-Phase 95W-130W )

Controller:uP6212 ( 2-Phase )

## ACPI:

UPI

## Other:

SATA(SATA2-300MB/s) \*6

SATA(JMB363 SATA2-300MB/s) \*1

ESATA(JMB363 SATA2-300MB/s) \*1

USB2.0 \*12 (Rear\*6 Front\*6)

NEC uPD720200 USB3.0 \*

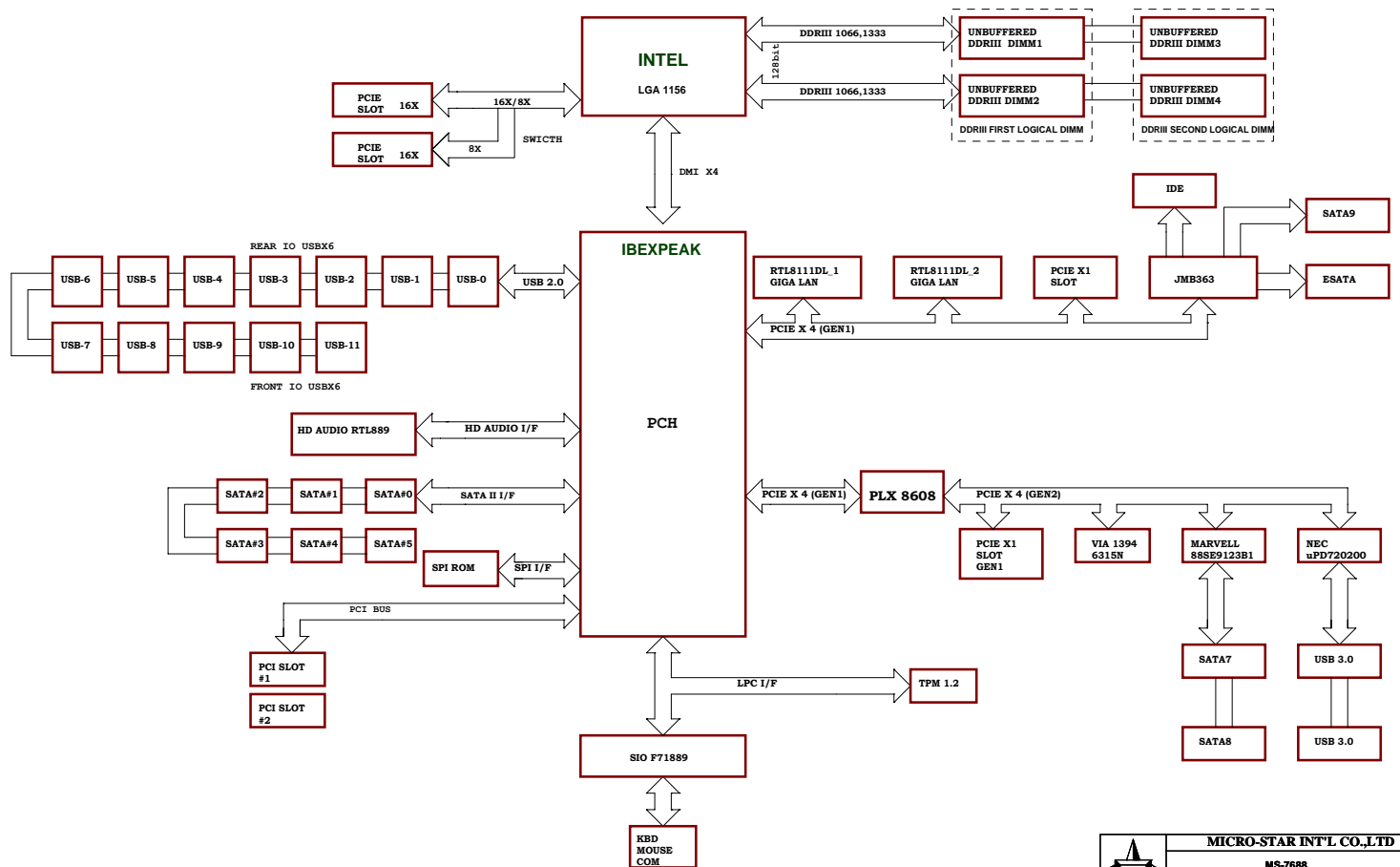
MARVELL SATA 6G\*2

1394 Controller - VT6315N-CE

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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

PCI Config.


DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#E PCI_INT#F PCI_INT#G PCI_INT#H	PCI_REQ0# PCI_GNT0#	AD16	CLK33M_PCISLOT_J20
TPM				LPCCCLK0
SIO				LPCCCLK1

TABLE 9:  
USB PORT MAPPING **(SUBJECT TO CHANGE)**

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
• UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
• UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
• UHCI #3, EHCI #1	Port 4	Front VIO	Yes	Yes	No	Yes
	Port 5	Front VIO	Yes	Yes	No	Yes
• UHCI #4, EHCI #2	Port 6	Front VIO	Yes	Yes	Yes	Yes
	Port 7	Front VIO	Yes	Yes	Yes	Yes
• UHCI #5, EHCI #2	Port 8	Rear VIO	Yes	Yes	Yes	Yes
	Port 9	Rear VIO	Yes	Yes	Yes	Yes
• UHCI #6, EHCI #2	Port 10	Rear VIO	Yes	Yes	Yes	Yes
	Port 11	Rear VIO	Yes	Yes	Yes	Yes
	Port 12	Rear VIO	Yes	Yes	Yes	Yes
• UHCI #7, EHCI #3	Port 13	Rear VIO	Yes	Yes	Yes	Yes

PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCIRST#	PCISLOT1
PE_RST#	TPM_RST#
PE_RST#	LPC/SIO



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BEXPEAK GPIO DEFINITION					SIO9 PIN ASSIGNMENT (UPDATE PENDING)				
Pin	GPIO	POWER WELL	IO	Function	Implementation	Pin	Pin Name	Function	Implementation
AK41	GPIO1	MAIN	1	BMBS12V	Pull-up to +3.3V and connect to the PECL REQ# pin (TRD) on the SIO	1	PWBTIN#	PWRBTN#	Connect to front panel header's power button pin
AL14	GPIO1	MAIN	1	IACH1	Through a 0.0 series resistor, connect to one of the front fan's TACH interface circuit	2	SLP_S3#	SLP_S3#	Connect to ICH10's SLP_S3# signal
AU8	GPIO2	MAIN	1	ICL_BQ0#	See PCA Spec	3	SLP_S5#	S4_STATE#	Connect to ICH10's S4_STATE# signal
AH7	GPIO3	MAIN	1	ICL_BQ0#	See PCA Spec	7	PDS_EN	CPU_FAN_TACH	Connect to the CPU fan tach interface
AP12	GPIO4	MAIN	1	ICL_BQ0#	See PCA Spec	8	COLOR	LED_PWR_COLOR	Controls the Power LED color
AW4	GPIO5	MAIN	1	ICL_BQ0#	See PCA Spec	10	PWBTOUT#	PWRBTN_OUT#	Connect to ICH PWRBTN# input
AV11	GPIO6	MAIN	1	IACH2	Pull-up to +3.3V and connect to P52-pin 12. The COMM B assembly connects pin 12 directly to GND	11	PS_ON#	PS_ON#	Connect to the appropriate power supply circuit
AW11	GPIO7	MAIN	1	IACH3	Through a 0.0 series resistor, connect to one of the front fan's TACH interface circuit	13	BLINK_GR	LED_PWR_BLINK	Connect to PS 2 through 68 ohm series resistor.
AX20	GPIO8	RESUME	0	IOX_5M#	Reserved	14	SKOPME#	RING#	Connect to ICH8 R#
AL28	GPIO9	RESUME	1	OC#	Associated with USB port 05 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	17	CLAMP_CTRL	CLAMP_CTRL	Use for clamping PCA voltage rails to decrease rail decay time
AL30	GPIO10	RESUME	1	OC#	Pull-up to +3.3VSB and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	28	SMB1SCL	SMB_CLK_MAIN	Connect to the clock signal of the main powered system SMBus
AL31	GPIO11	RESUME	1	SMBALERT#	Pull-up to +3.3VSB. It is always enabled as a wake event	29	SMB2SCL	SMB_CLK_STDBY	Connect to the clock signal of the standby powered system SMBus
AF74	GPIO12	RESUME	1	LAM_DISABLE	Follow implementation in Intel Pkinton Design Guide	33	GPSRST#	PCI_EXP_RST#	Use to reset all the PCIe devices and slots
AR16	GPIO13	RESUME	1	IO_PME	Pull-up to +3.3V SB and connect to P151-pin 10; also add a no-installed pull-down to the net.	34	FANPWM2	CHAS_FAN_PWM	Connect to the Chassis Fan PWM interface
AM00	GPIO14	RESUME	1	OC#	Pull-up to +3.3VSB and connect to the SMI pin on the SIO	35	GPIO25	PWM_IN	Connect to the ICH10's PWM0 output - NEW for Eaglelake
AT36	GPIO15	RESUME	1	IOH_CP15	Reserved	36	PME_IN#	P_PME#	Connect to the PME# pin of the ICH10
AP09	GPIO16	RESUME	0	SATAACP	Follow implementation in Intel Pkinton Design Guide	37	USB_PWR#	USB_PWR#	Input to USB Power control, connect to the ICH10's SLP_S5# signal
AW11	GPIO17	MAIN	1	IACH4	Through a 0.0 series resistor, connect to one of the front fan's TACH interface circuit	38	SV_SW_MAIN#	SV_DUAL_CTRL	Connect to control inputs of dual rail switches
AP09	GPIO18	MAIN	1	PCIECLK0#	Through a 1KΩ series resistor, pull-up to +3.3V and connect to E16-pin 1.	39	EVENT6#	PCI_EXP_WAKE#	Connect to WAKE# pins of PCIe devices and slots
AP09	GPIO19	MAIN	1	SATAACP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	47	PDS_EN2	PDS_EN2	Use as control signal for appropriate voltage regulators
AP08	GPIO20	MAIN	1	PCIECLK02#		48	CPU_PSRNT1#	SKTOCC#	Connect to SKTOCC# on CPU
AT37	GPIO21	MAIN	1	SATAACP	Pull-up to +3.3V and connect to P23-pin 4.	49	WAKE_OUT#	ICH_WAKE#	Connect to the ICH10's WAKE# input
AM41	GPIO22	MAIN	1	SLDLOC	Pull-up to +3.3V and connect to P150-pin 10	50	GPIO14	HOOD_UNLOCK#	Connect to P124 pin 1 and a 2.2K pull-up to +5V.
AP14	GPIO23	MAIN	1	LDREQ#	Pull-up to +3.3V and connect to the PCI SLOTT Rise Detect circuit	51	GPIO16	HOOD_UNLOCK#	Connect to P124 pin 6 and a 2.2K pull-up to +5V.
AR04	GPIO24	RESUME	0	MEMLED	Through a 1KΩ series resistor, pull-up to +3.3VSB and connect to P125-Pin 1	53	AUDIO_BEEP	DIAG_BEEP	Connect to the system's integrated audio solution
AP33	GPIO25	RESUME	1	PCIECLK03#		54	FANPWM1	CPU_FAN_PWM	Connect to the CPU fan's PWM circuit
AP37	GPIO26	RESUME	1	PCIECLK04#		55	GPIO35	PECL_REQ#	Connect to the ICH10's BM_BUS# signal - New for Eaglelake, C#IC4 support
AP37	GPIO27	RESUME	0	OD_PLL_VB_EN		56	HD_LED_IN#	SATA_LED#	Connect to the ICH10's SATA_LED# output signal
AV40	GPIO28	RESUME	0	IOH_CP28		58	HMSCL	HLTH_MON_CLK	Connect to CLK pin on SensorBus device
BA35	GPIO29	RESUME	0	SLP_LAN#	Connect to a circuit used to force the 3.3V_CL rail on.	59	HMSDA	HLTH_MON_DAT	Connect to DAT pin on SensorBus device
AT37	GPIO30	RESUME	1	SUS_PWR_ACK		60	GPIO10	PLPY_DRVEN	Use in floppy implementation
AP00	GPIO31	MAIN	1	ACPRESENT	TBD. For now connect to a Test Point	61	HD_LED_OUT#	HD_LED#	Connect to the front panel HDD LED
AL40	GPIO32	MAIN	0	IOH_CP32	Through a 1KΩ series resistor, pull-up to +3.3V and connect to P1-pin 20.	100	SMB1SDA	SMB_DATA_MAIN	Connect to the data signal of the main powered system SMBus
AL16	GPIO33	MAIN	0	IOH_CP33	Through a 1KΩ series resistor, pull-up to +3.3V and connect to pin 1 of JUMP# E1	101	SMB2SDA	SMB_DATA_STDBY	Connect to the data signal of the standby powered system SMBus
AL40	GPIO34	MAIN	0	SP_PCH	Pull-down to GND and connect to P124-pin 2. Decouple with 0.1μF	102	SV_USB_MAIN#	SV_USB_MAIN#	Connect to the control pin of the SV_DUAL circuit.
AR41	GPIO35	MAIN	0	SATACLKREQ#	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	103	GPIO41	PS_FAN_TACH	Where applicable, connect to power supply's fan tach circuit.
AP09	GPIO36	MAIN	1	SATAACP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	104	FANPWM3	PS_FAN_PWM	Where applicable, connect to the power supply's fan PWM circuit
AL18	GPIO37	MAIN	1	SATAACP	Pull-up to +3.3V and connect to P125-pin 16	105	PWRGD_01	PWRGD_30MS	Use for appropriate system board sequencing
AP08	GPIO38	MAIN	1	SLDAD	Through a series 1K resistor, connect to P5-pin 9 and pull-up to +3.3V	106	PWRGD_02#	PWRGD_30MS#	Use for appropriate system board sequencing
AL39	GPIO39	MAIN	1	SDATAOUT0	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	110	FAN_TACH1	CHAS_FAN_TACH	For systems with a chassis fan, connect to the chassis fan TACH circuit
AL30	GPIO40	RESUME	1	OC1	Using an 8.2KΩ resistor, pull-down to GND and connect to E49-pin 2	111	SM1#	LPC_SM1#	Connect to appropriate ICH10 SM1-capable GPIO, reference ICH10 GPIO matrix
AX28	GPIO41	RESUME	1	OC2	Associated with USB port 2 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	120	R1Z#	R1Z#	Where applicable, connect to appropriate serial port pin
AP30	GPIO42	RESUME	1	OC3	Associated with USB port 3 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	122	DCD2#	DCD2#	Where applicable, connect to appropriate serial port pin
AP31	GPIO43	RESUME	1	OC4	Associated with USB port 4 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	123	S1N2	S1N2	Where applicable, connect to appropriate serial port pin
AW18	GPIO44	RESUME	1	PCIECLK05#		124	SOUT2	SOUT2	Where applicable, connect to appropriate serial port pin
AV36	GPIO45	RESUME	1	PCIECLK06#		125	DSR2#	DSR2#	Where applicable, connect to appropriate serial port pin
AF36	GPIO46	RESUME	1	PCIECLK07#		126	RTS2#	RTS2#	Where applicable, connect to appropriate serial port pin
AV39	GPIO47	RESUME	1	PEG_A_CLKRQ#		127	CTS2#	CTS2#	Where applicable, connect to appropriate serial port pin
AC38	GPIO48	MAIN	1	SDATAOUT1	Pull-up to +3.3V and connect to P24-pin 10	128	DTR_BOUT2#	DTR2#	Where applicable, connect to appropriate serial port pin
AC40	GPIO49	MAIN	0	SATAACP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.				
AW5	GPIO50	MAIN	1	ICL_REQ#1	Use as REQ1#.				
AB6	GPIO51	MAIN	0	ICL_GNT#1	Use as GNT1#.				
AV14	GPIO52	MAIN	1	ICL_REQ#2	Pull-up to +3.3V				
BA9	GPIO53	MAIN	0	ICL_GNT#2	Connect to TP				
AP48	GPIO54	MAIN	1	ICL_REQ#3	Through a 8.2KΩ series resistor, connect to P14-pin 2 and pull-down to GND.				
AM3	GPIO55	MAIN	0	ICL_GNT#3					
AW5	GPIO56	RESUME	1	PEG_B_CLKRQ#	Connect to circuit that controls the amplifier's output.				
AL32	GPIO57	MAIN	1	IOH_CP57	Pull-up to +3.3VSB				
AV71	GPIO58	RESUME	0	SMLCLK	Associated with USB port 0 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.				
AT31	GPIO59	RESUME	1	OC#					
BA33	GPIO60	RESUME	0	SMLALERT#					
AK31	GPIO61	RESUME	0	SUS_STAT#	Power Down for external TPM				
AP11	GPIO62	RESUME	0	SUSCLK	SUSCLK to SIO				
AV36	GPIO63	RESUME	0	SLP_5M#	Connect to USB Power Control on SIO				
AD10	GPIO64	MAIN	0	CLKOUTFLEX0					
AK1	GPIO65	MAIN	0	CLKOUTFLEX1					
AB6	GPIO66	MAIN	0	CLKOUTFLEX2					
AL3	GPIO67	MAIN	0	CLKOUTFLEX3					
AV34	GPIO72	RESUME	1	IOH_CP72	Through a series 1KΩ resistor, pull-up to +3.3VSB and connect to P5-pin 10.				
AN35	GPIO73	RESUME	1	PCIECLK08#					
AY32	GPIO74	RESUME	0	SMLALERT#					
AB31	GPIO75	RESUME	0	SMLDATA					

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GPIO Table

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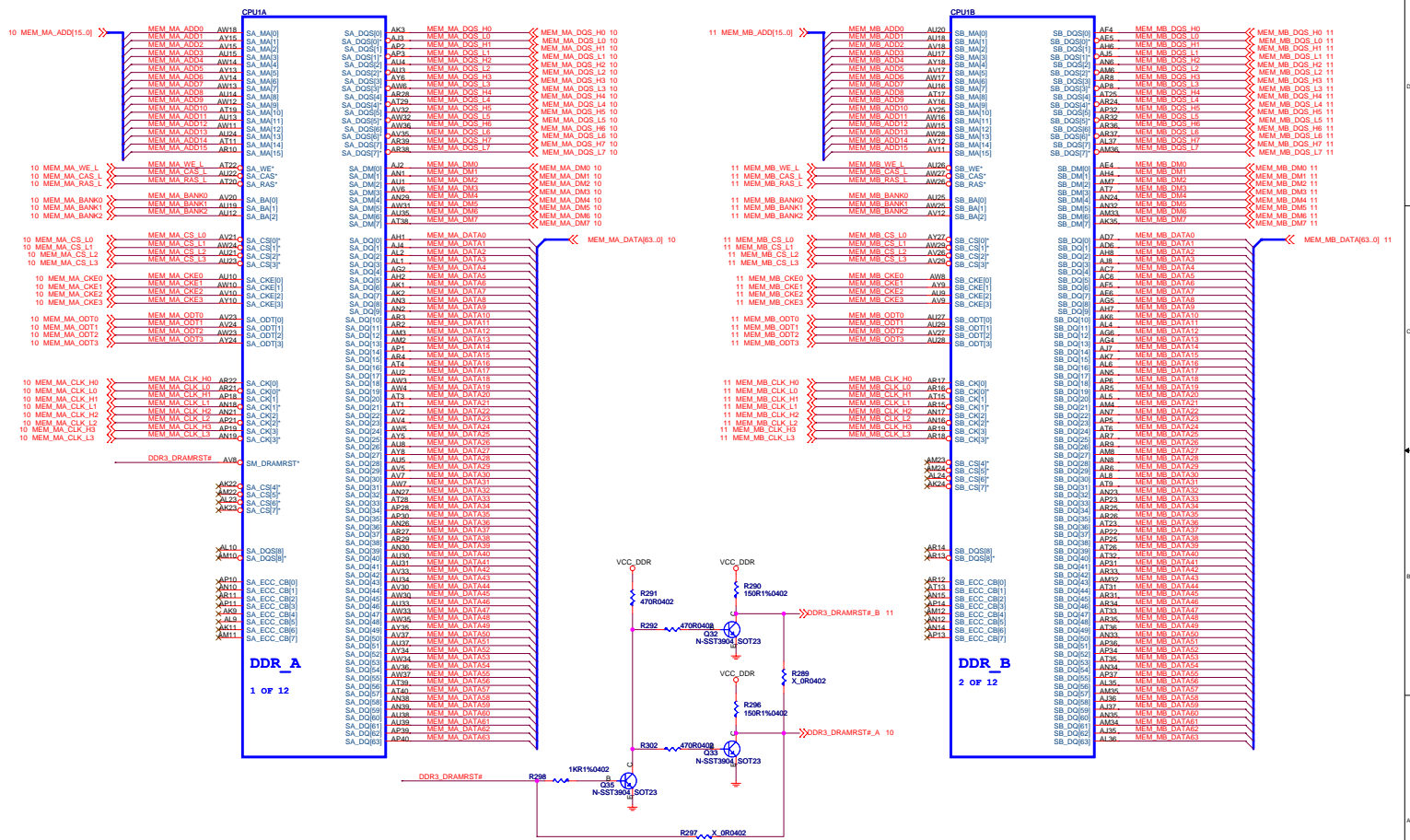
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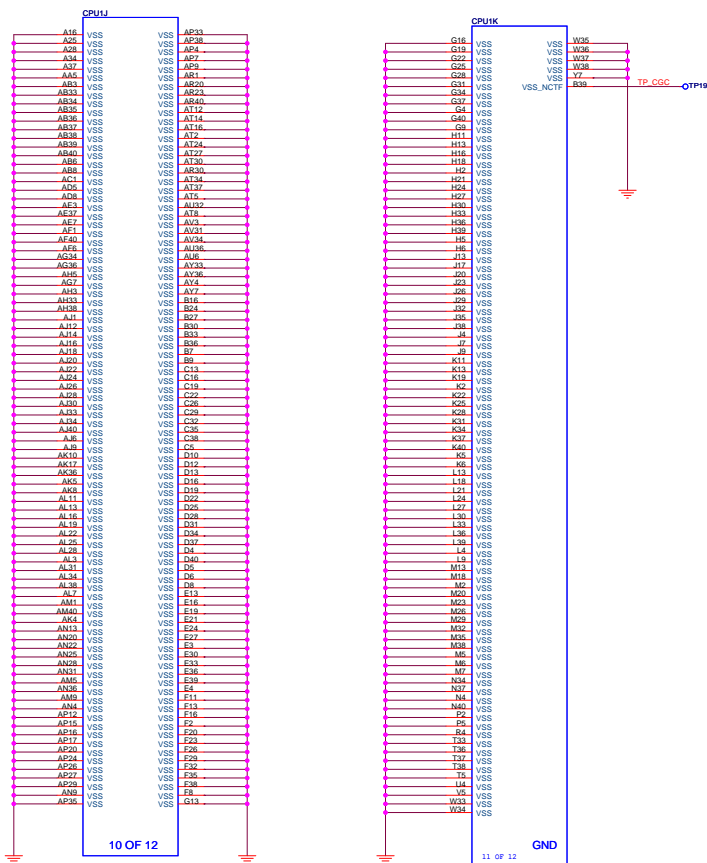
		
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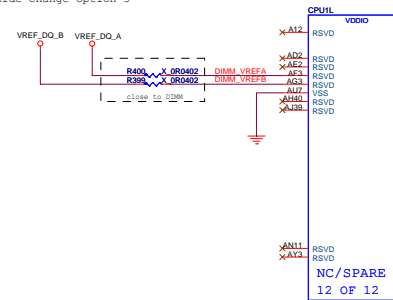






NOTE:R378,R461 STUFFED,IF DDR3 DIMM VREFDQ OPTION 2 UNSTUFFED.

FOLLOW DDR3 DIMM VREFDQ Platform Design  
Guide Change Option 3



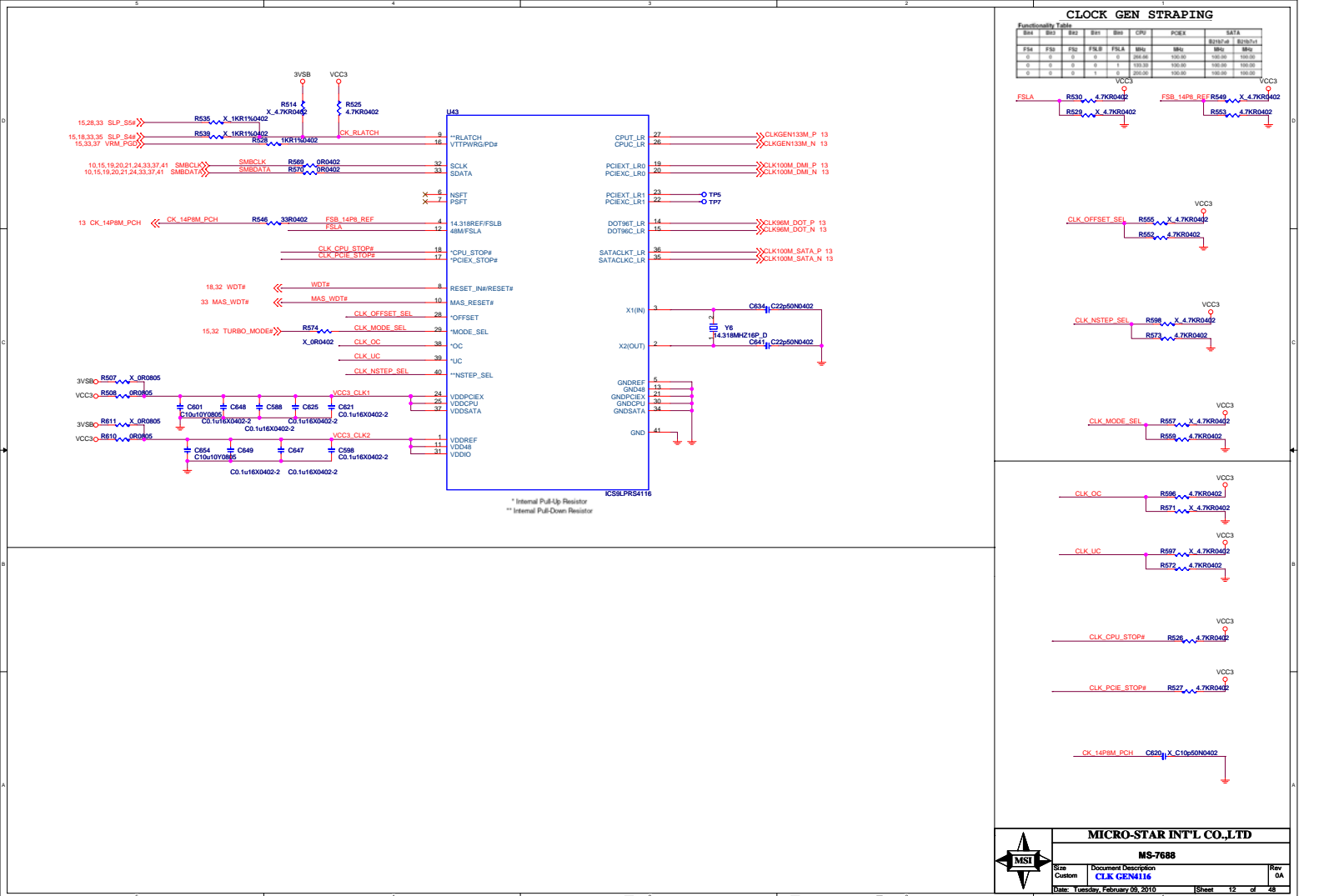
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## DDRIII DIMM\_A2



## DDRIII DIMM B2

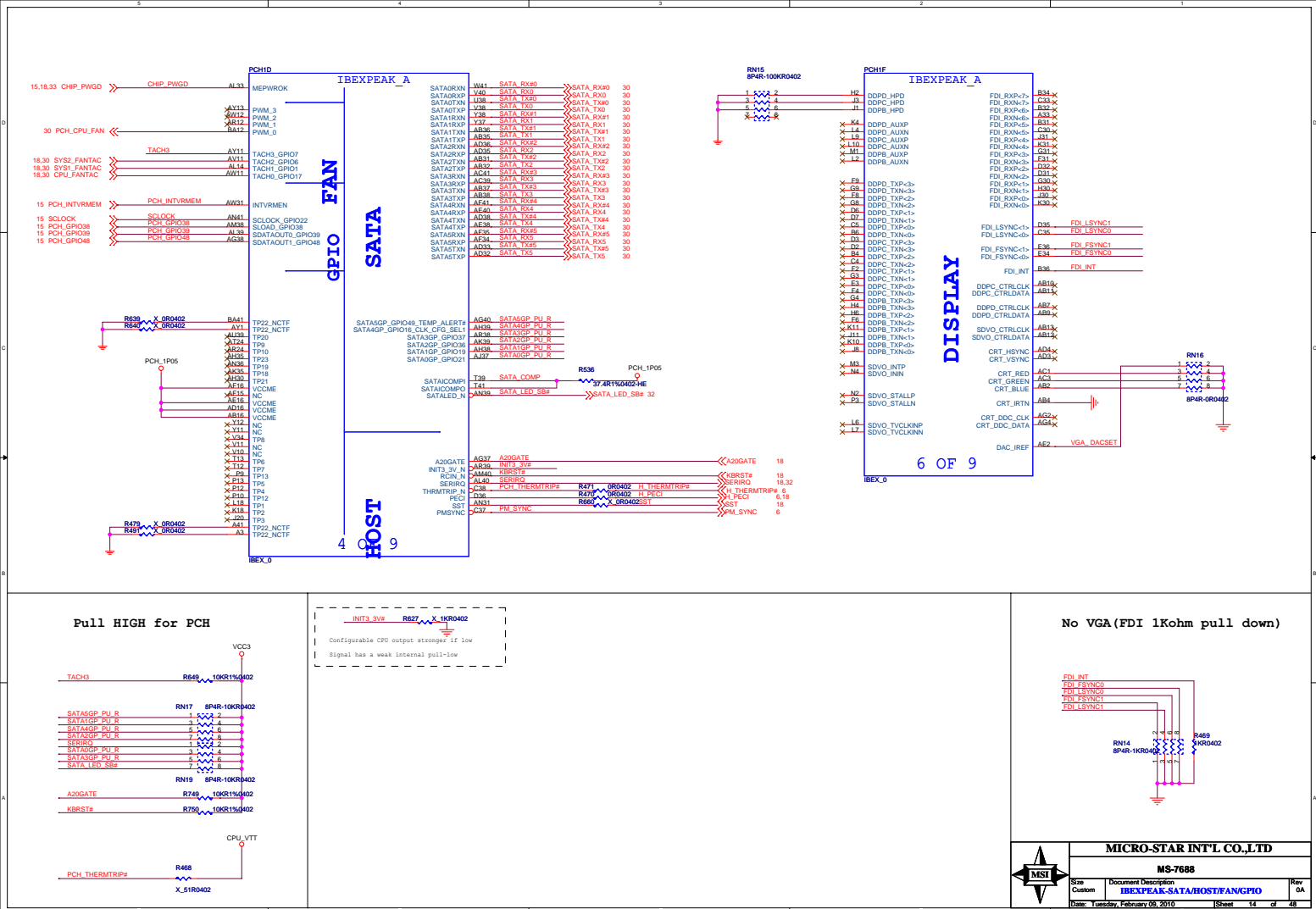




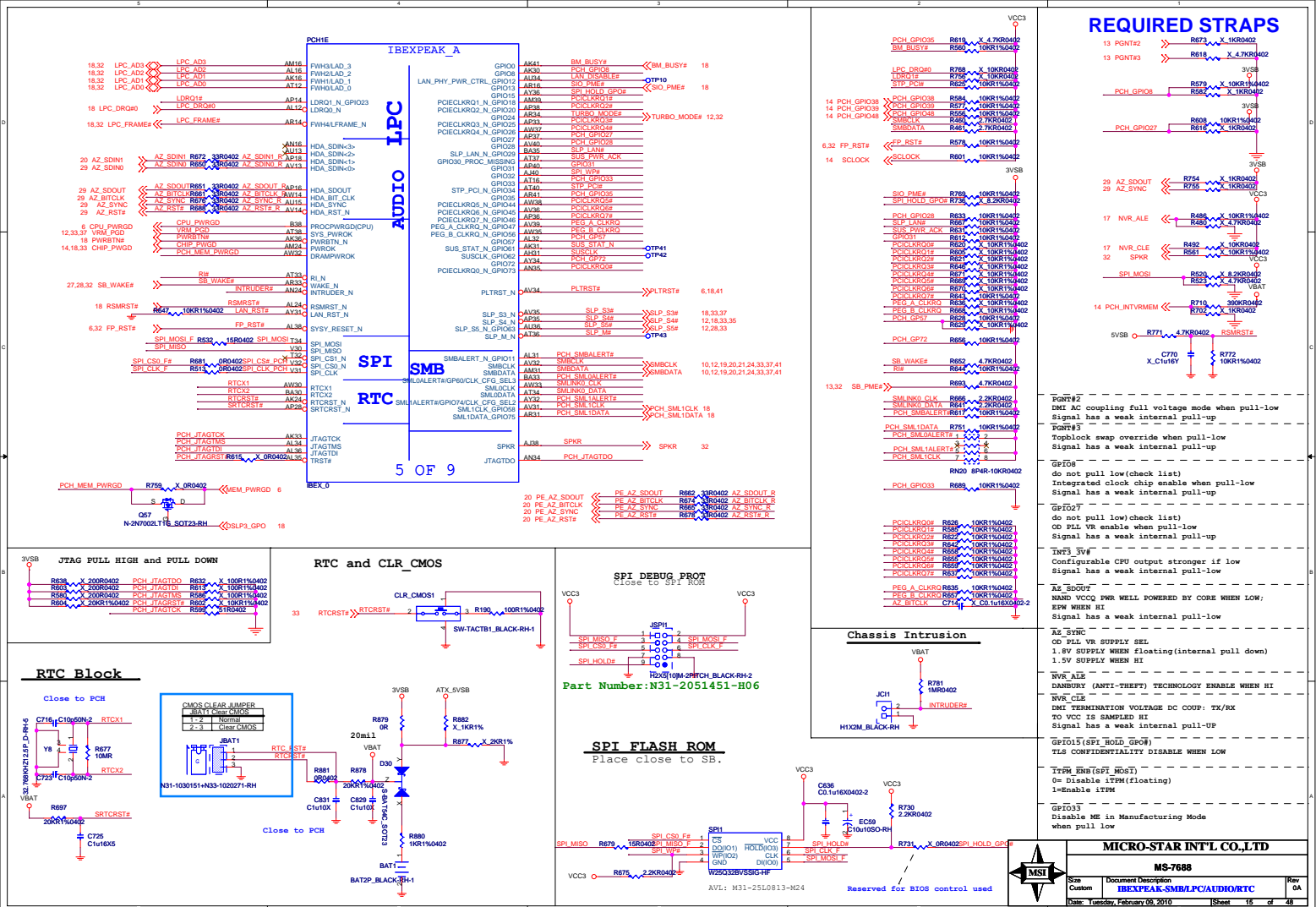
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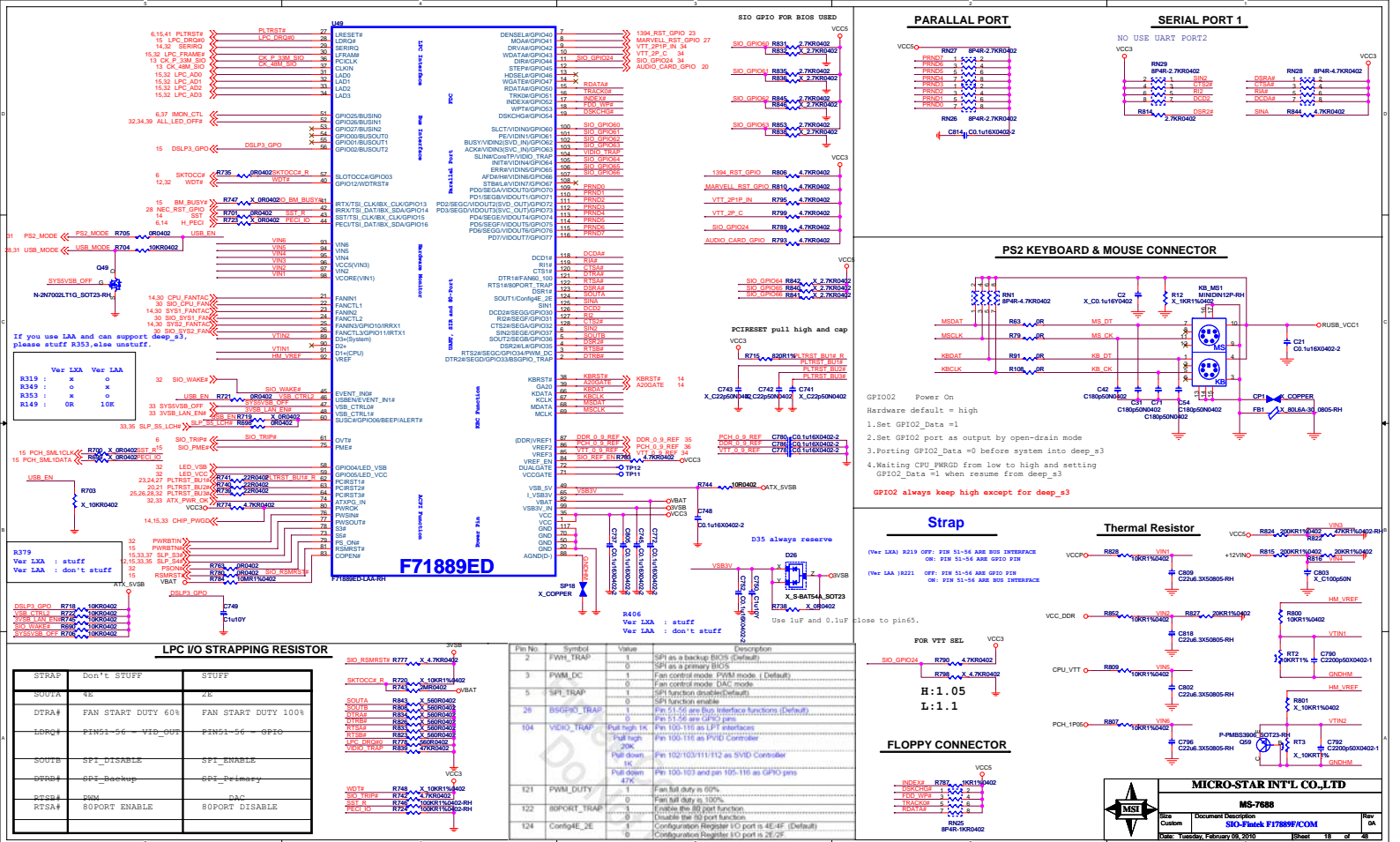
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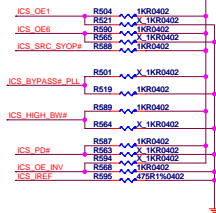
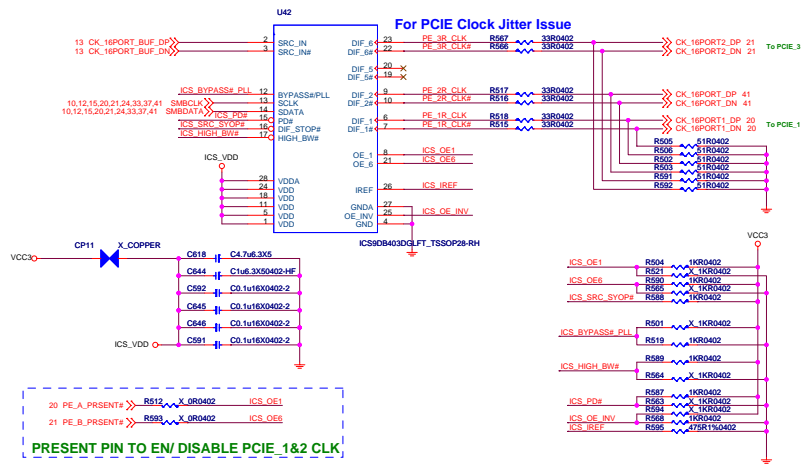
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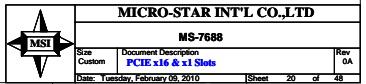
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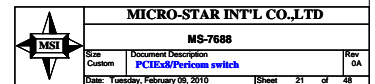
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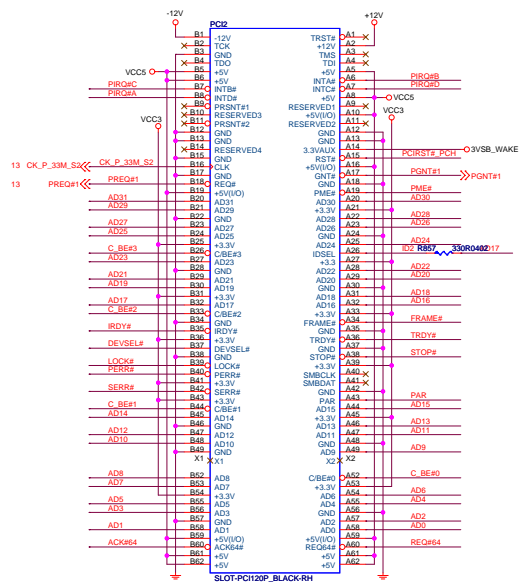




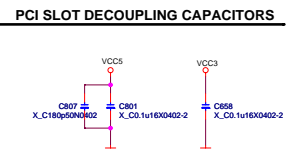
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PCI SLOT 2 (PCI VER: 2.2 COMPLY)



```
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B
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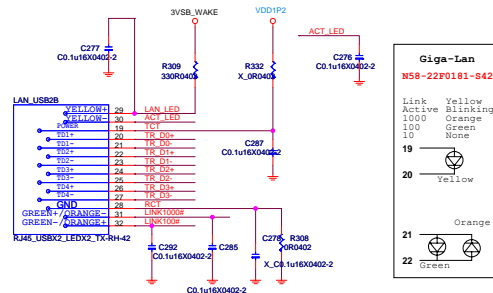
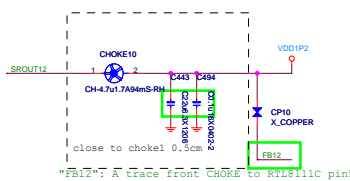
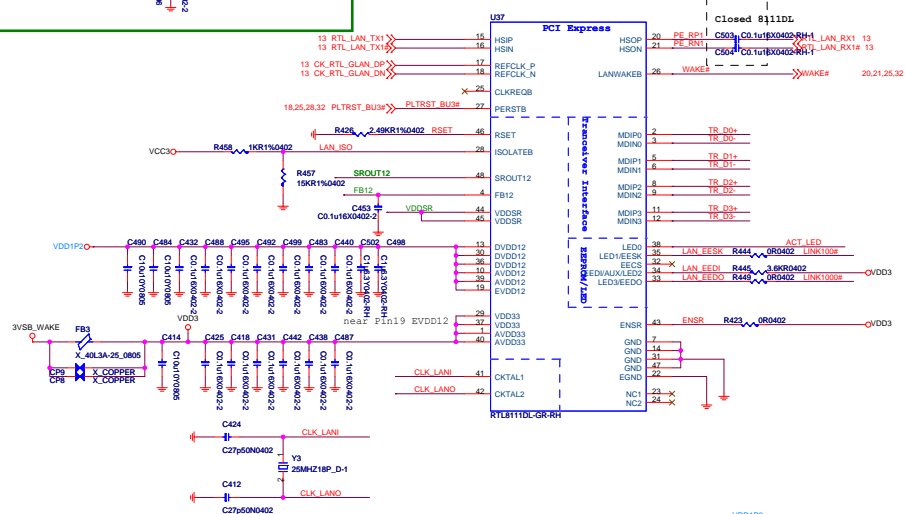
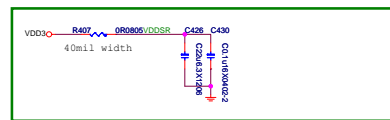
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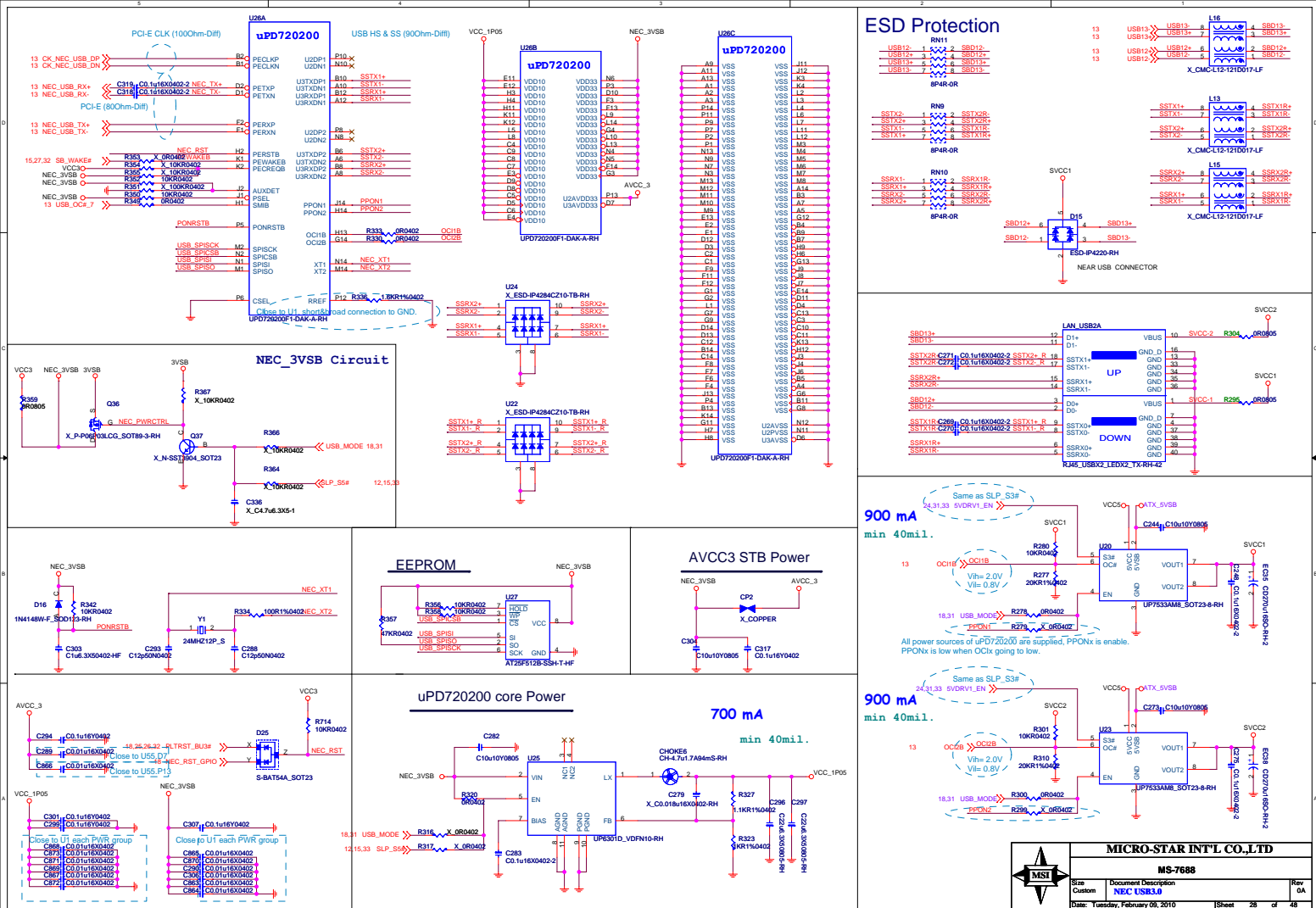






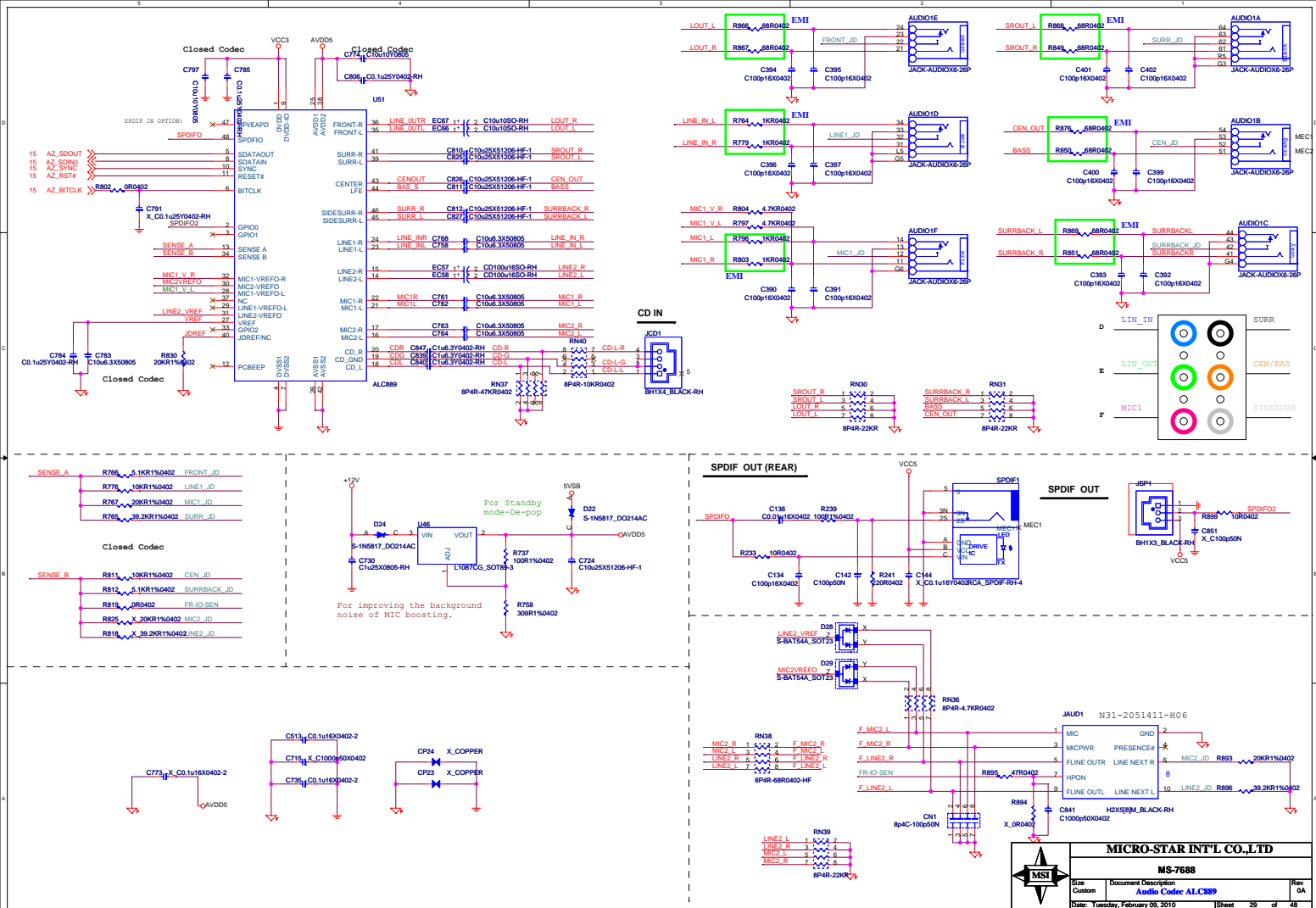






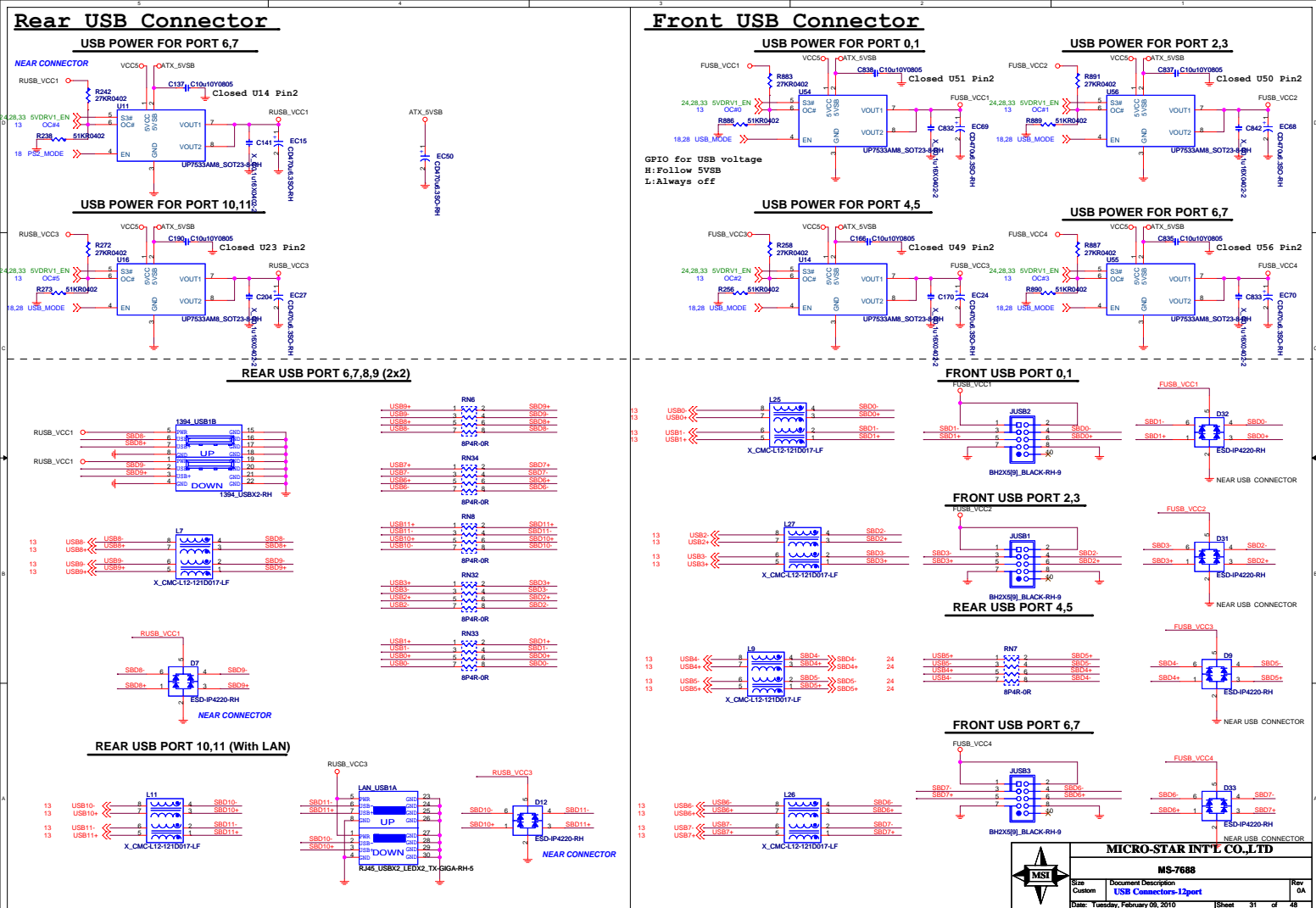
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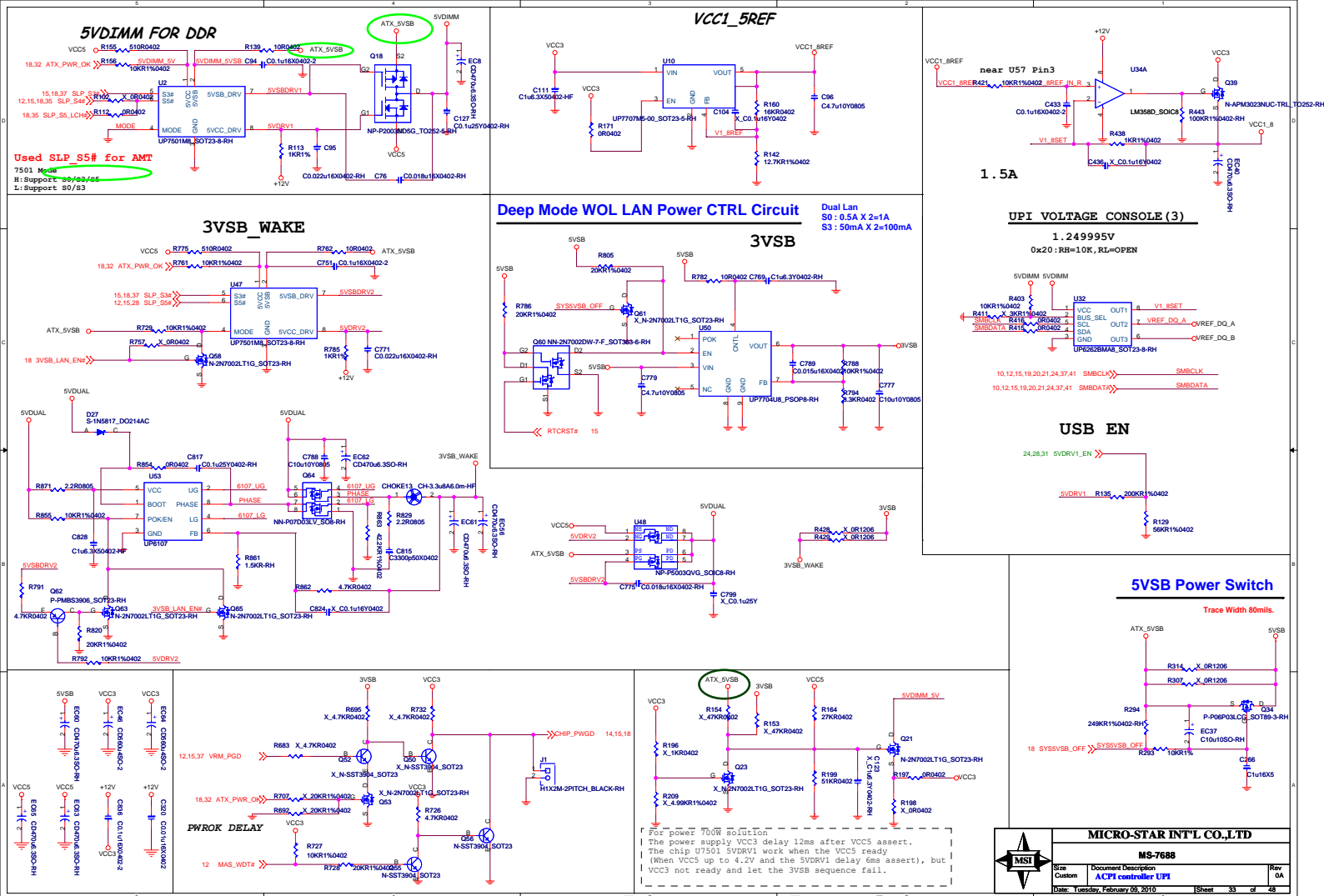


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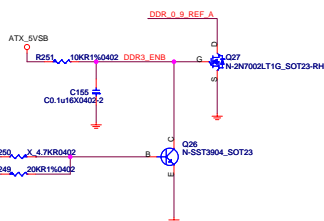




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```
SIO      虫瑯 0.9VREF
6264     虫瑯 1.5VREF
```



### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

The diagram illustrates the DDR VTT Power circuit. It shows the connection from 5VBB and VCC5 to the DDR VTT power plane. The circuit includes resistors R236, R237, R243, and R244, capacitors C140, C139, and CEC7, and a DP7711U1M PSOP08RH component. The diagram also shows the connection to the DDR VTT power plane and the VTT\_DOR signal.

Key components and connections:

- 5VBB** and **VCC5** are connected to the circuit.
- R236** (X\_OR0805) and **R237** (GR0805) are connected to the 5VBB and VCC5 pins.
- U12** (DP7711U1M PSOP08RH) is connected to the circuit.
- VREF2**, **ENABLE**, **VOUTL**, **BOOT\_SEL**, and **VOUT** are connected to the U12 pins.
- VIN**, **GND**, **VDD**, and **GND** are connected to the U12 pins.
- VDD\_VREF** is connected to the U12 pin.
- VDD\_VREF** is connected to the **DDR\_VTT\_VREF** pin.
- R243** (1KR150402) and **R244** (1KR150402) are connected to the VDD\_VREF pin.
- C140** (1u25X0805-RH) and **C139** (1u25X0805-RH) are connected to the VDD\_VREF pin.
- CEC7** (0.025X0805-RH) is connected to the VDD\_VREF pin.

Calculated value:  $0.2075A^4 = 0.8A$

	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7688</b>		
	Size Custom	Document Description <b>DDR Power - uP6103 1-Phase</b>	Rev 0A
	Date: Tuesday, February 09, 2011		ISheet 36 of 48



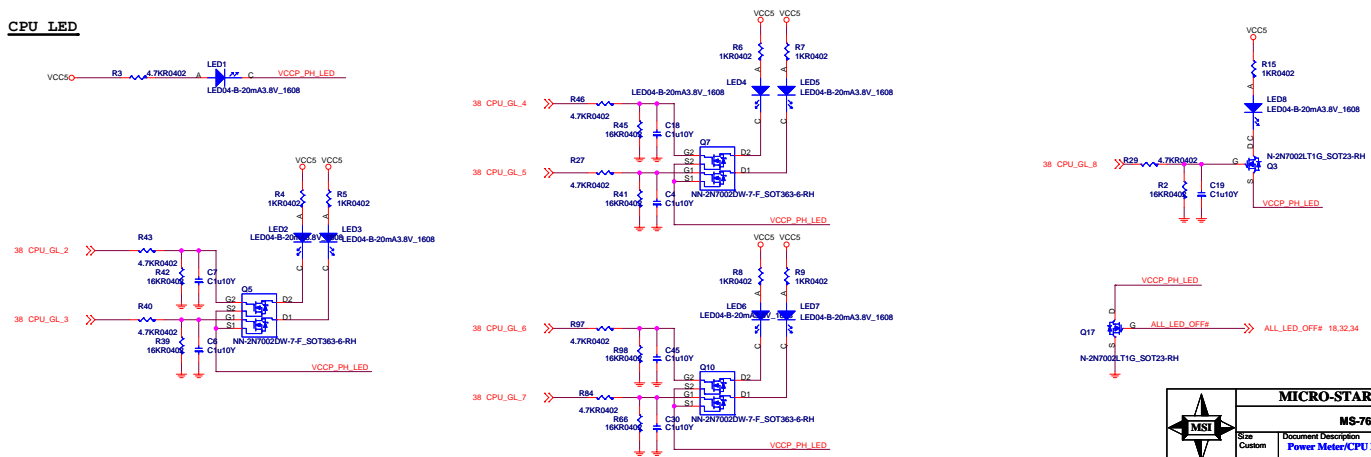


## VRMPWRGD LEVEL SHIFT





# CPU\_LED



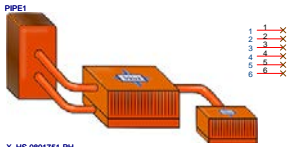
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MS-7688		
Size	Document Description	Rev
Custom	Power Meter/CPU LED CTL	0A
Date: Tuesday, February 09, 2010 [Sheet 39 of 48]		

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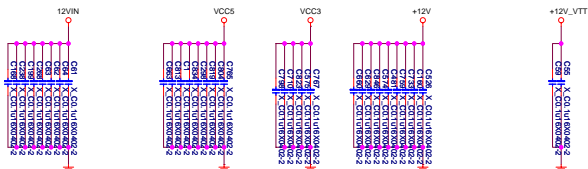
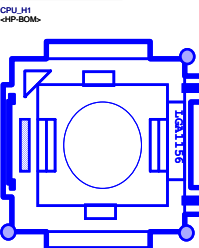




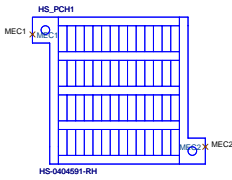
HEATPIPE



CPU SOCKET



HEATSINK



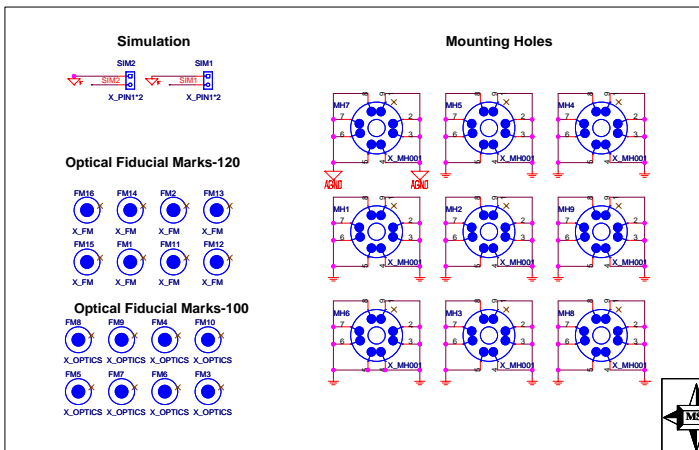
BATTERY



PCB



PD0-0758510-G37, 弘8, 23, 脚 吹邻红 (MSIS)  
PD0-0758510-G37, 弘8, 138, 脚 吹邻红 (MSIS)  
PD0-0758510-E55, 弘8, 23, 脚 吹邻红 (MSIS)  
PD0-0758510-E55, 弘8, 17, 脚 吹邻红 (MSIS)



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MS-7688			
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Custom	MSI_1_ECO_control	0A	
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